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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|------------------------|------------------------|------------------|
| 10/784,140 | 02/20/2004 | Michael David Mulligan | 50019.271US01/P05768 | 5361 |
| 23552 | 7590 | 02/03/2005 | EXAMINER | |
| MERCHANT & GOULD PC P.O. BOX 2903 MINNEAPOLIS, MN 55402-0903 | | | ZWEIZIG, JEFFERY SHAWN | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2816 | |

DATE MAILED: 02/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Applicati n No.

10/784,140

Applicant(s)

MULLIGAN, MICHAEL DAVID

Examiner

Jeffrey S. Zw izig

Art Unit

2816

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 February 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) _____ is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-20 is/are allowed.
- 6) ☒ Claim(s) 1-4, 6 and 10-15 is/are rejected.
- 7) ☒ Claim(s) 5, 7-10 and 16-20 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 November 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>8/16/04</u> . | 6) <input type="checkbox"/> Other: _____ |

Drawings

1. Figs. 1A and 1B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. It would appear that apparatus claims 13-20 should be method claims.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 6 and 10-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Torikoshi et al. (USPN 5,436,614).

Figs. 1 and 4 disclose an integrated circuit comprising a PTAT voltage temp sensor block 19, a level shifter block R4/Q providing a level shifted signal V(-), a gain block SW/R1-R3/OP with a gain providing an output signal A/D, an ADC A/D and a central logic block CPU providing a control signal to SW as recited in claims 1-3, 10 and 11.

Alternately, Figs. 1 and 7a/b disclose an integrated circuit comprising a PTAT voltage temp sensor block 19, a level shifter block (R4 & switches) providing a level shifted signal to a gain block Q with a gain providing an output signal A/D, an ADC A/D and a central logic block CPU providing a control signal to the switches as recited in claims 1-3, 10 and 11.

Further shown is a plurality of level shifter blocks R4 as recited in claim 4.

Further shown is an adjustable bias circuit R4 as recited in claim 6.

Claims 12-15 are anticipated for the reasons above.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1-4, 6 and 11-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hara et al. (USPN 5,140,302) in view of McCormack (USPN 3,790,910).

Hara et al. Fig. 1 disclose an integrated circuit comprising a PTAT voltage temp sensor block 1, a level shifter block R1-R3/Q1 providing a level shifted signal, an ADC 2b and a central logic block 2a providing a control signal to Q1 as recited in claims 1-3 and 11. Hara et al. does not appear to disclose the gain block recited in claim 1. McCormack discloses a similar circuit including gain block 50. It would have been obvious to one of ordinary skill in the art at the time of the invention modify the Hara et al. circuit with a gain block as taught by McCormack for the benefit of current isolating the ADC from the temp and level shifter blocks. Claims 1-3 and 11 are obvious. Note, Frazier and Nakamura also teach the benefits of using gain blocks to isolate ADCs from preceding blocks.

Further shown is a plurality of level shifter blocks R1/R3 as recited in claim 4.

Further shown is an adjustable bias circuit R1/R3 as recited in claim 6.

Claims 12-15 are anticipated for the reasons above.

Conclusion


7. Claims 5, 7-10 and 16-20 are objected to as being dependent upon a rejected base claim, but may be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey S. Zweizig whose telephone number is (571) 272-1758. The examiner can normally be reached on Monday thru Thursday 6:00 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Jeffrey S. Zweizig
Primary Examiner
Art Unit 2816

JZ